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EXAMINER	
VERDERAMO III, RALPH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,729	LANDIN ET AL.	
	Examiner	Art Unit	
	RALPH A. VERDERAMO III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,16-25 and 28-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 16-25 and 28-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 4, 16, 18, 19, 28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over “The Sun Fireplane System Interconnect” by Alan Charlesworth (herein after referred to as Alan) in view of The Cache Memory Book by Jim Handy (herein after referred to as Jim).

Regarding claims 1, 16 and 28, Alan describes a system, comprising: an inter-node network (SSM Interconnect of FIG. 3 connecting snooping coherence domains (nodes)); and a plurality of nodes coupled by the inter-node network (multiple snooping coherence domains (nodes) are connected through the SSM Interconnect shown in FIG. 3 also explained in sec. 3 on page 3 referring to Large Fireplane systems), wherein each of the plurality of nodes includes a

plurality of active devices (processors in the snooping coherence domain (node) of FIG. 3), an interface configured to send and receive coherency messages on the inter-node network (SSM Agent of FIG. 3), and an address network coupling the plurality of active devices to the interface (The bus shown in the snooping coherence domain of FIG. 3); wherein an active device included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending a remote write back (RWB) address packet on the address network if the active device is included in a multi-node system (Remote_WriteBack request which occurs when there is a request to get a write back done in another snooping coherence domains (multiple nodes) (page 5, sec. 6.2). Remote data is only possible in Large Fireplane systems using multiple snooping coherence domains (nodes) (page 3, sec 3)), and a write back (WB) address packet on the address network if the active device is included in a single node system (WriteBack request (page 5, sec. 6.1) which occurs when there is a request to write back inside a snooping coherence domain (also in a Mid-size Fireplane system where there is only a single snooping coherence domain (node) (page 3, sec. 3))). Alan does not specifically describe wherein each active device included in the node having access to or ownership of the coherency unit is configured to ignore the RWB address packet or the situation of if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before an interface included in the node sends a responsive address packet, the other active device

is configured to provide data to the interface in response to the responsive address packet.

Alan does describe how during a remote transaction the local CPU's (active devices) ignore the transaction (page 7, sec. 8.2). Examiner believes that since the Remote_WriteBack is a remote transaction it would have been obvious to one of ordinary skill in the art at the time of the invention that a Remote_WriteBack would operate in a similar matter as the described remote transaction and therefore the local CPU's would ignore the Remote_WriteBack. Alan still does not specifically describe the situation of if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before an interface included in the node sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet.

Jim describes the MESI protocol (pages 156 - 158 of The Cache Memory book, provided as pages 1 - 3 of NPL). It is described that if one cache has an Exclusive or Modified line (owned), all matching lines in other caches would have been marked invalid. In these states no other location has a copy of the data. Therefore if another active device were to acquire data in an Exclusive or Modified state all further requests to that data would have to be provided from that active device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a MESI protocol as described by Jim with the

invention of Alan because MESI is a conventional cache coherency protocol which maintains coherency of cache lines between processors.

Regarding claims 3, 18 and 30, Alan in view of Jim describe the system of claim 1 (see above), the node of claim 16 (see above) and the method of claim 28 (see above), wherein the active device is configured to send the RWB address packet if the active device is included in a multi-node system and if the coherency unit is not mapped by any memory subsystem included in the node (Remote data is only possible in Large Fireplane systems using multiple snooping coherence domains (nodes) (Alan, page 3, sec. 3). Furthermore, Alan describes that requests for remote data are issued for non-local physical addresses (Alan, page 5, sec. 6.2). If the data is at a non-local physical address it is therefore not mapped by any memory subsystem included in the node).

Regarding claims 4, 19 and 31, Alan in view of Jim describes the system of claim 3 (see above), the node of claim 18 (see above) and the method of claim 30 (see above), wherein an interface included in the node (SSM Agent of FIG. 3) is configured to send a coherency message via the inter-node network to a home node for the coherency unit in response to receiving the remote write back address packet (Remote_WriteBack request the local SSM agent to get a WriteBack done in another snooping coherence domain (node) (Alan, page 5, sec. 6.2)). While it is not specifically described that each active device in the node ignores the RWB address packet, Alan does describe how during a remote transaction the local CPU's (active devices) ignore the transaction (page 7, sec.

8.2). Examiner believes that since the Remote_WriteBack is a remote transaction it would have been obvious to one of ordinary skill in the art at the time of the invention that a Remote_WriteBack would operate in a similar matter as the described remote transaction and therefore the local CPU's would ignore the Remote_WriteBack.

4. Claims 2, 17 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alan in view of Jim as applied to claims 1, 16 and 28 above, further in view of McCracken et al. US Patent No. 6381681 (herein after referred to as McCracken).

Regarding claims 2, 17 and 29, Alan in view of Jim describe the system of claim 1 (see above), the node of claim 16 (see above) and the method of claim 28 (see above). They do not specifically describe wherein each active device included in the node having access to or ownership of the coherency unit is configured to transition an access right or an ownership responsibility for the coherency unit in response to the second type of address packet.

McCracken describes that release operations include any operation that causes a processor to no longer own a cache line such as write backs (column 4, lines 46 – 48). Therefore if a processor (CPU or active device) requests a write back it will no longer own the cache line (coherency unit) (transition access right or an ownership responsibility).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have transitioned access rights to or an ownership responsibility for a coherency unit in response to a write back as described by McCracken with

the invention of Alan in view of Jim because McCracken shows that a write back operation results in a processor no longer owning a cache line (column 4, lines 46 - 48).

5. Claims 5 - 9, 20 - 23 and 32 - 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Alan in view of Jim as applied to claims 4, 19 and 31 above further in view of Hagersten US Patent Application Publication No. 2001/0051977 (herein after referred to as Hagersten).

Regarding claims 5 and 32, Alan in view of Jim describe the system of claim 4 (see above) and the method of claim 31 (see above). While they do describe a remote write back transaction, they do not specifically describe wherein a home interface in the home node is configured to lock the coherency unit in response to the coherency message and to responsively send an additional configured message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node.

Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to write the coherency unit back (responsively send an additional coherency message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169]). Alan describes the interfaces used to send and receive such inter-node messages (SSM Agents of Alan FIG. 3). Furthermore while

Hagersten does not explicitly describe that the coherency unit is locked in response to the received coherency message it would have been obvious to one of ordinary skill in the art at the time of the invention to do so because coherency should be protected when transactions that have an affect on the coherency have not completed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the steps for accomplishing a write back as described by Hagersten with the invention of Alan in view of Jim because Hagersten shows that a write back request is performed in such a way (page 13, paragraph [0169]).

Regarding claims 6 and 33, Alan in view of Jim and Hagersten describe the system of claim 5 (see above) and the method of claim 32 (see above), wherein in response to receiving the additional coherency message, the interface in the node is configured to send a proxy read-to-own-modified address packet on the address network (Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to write the coherency unit back (responsively send an additional coherency message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169]). Alan describes the interfaces used to send and receive such inter-node messages (SSM Agents of Alan FIG. 3)).

Regarding claims 7, 21 and 34, Alan in view of Jim and Hagersten describe the system of claim 6 (see above), the node of claim 20 (see below) and the method of claim 33 (see above), wherein each active device included in the node having an access right to the coherency unit and not having an ownership responsibility for the coherency unit is configured to invalidate the access right in response to the proxy read-to-own-modified address packet (Alan describes that cache tags represent the actual state of the data in the cache and consequently they transition with the data transfer or data modification (page 4, sec. 4.3 and 4.3.1). Since data is being transferred to the home node for write back the state should be invalid).

Regarding claims 8, 22 and 35, Alan in view of Jim and Hagersten describe the system of claim 6 (see above), the node of claim 20 (see below) and the method of claim 33 (see above), wherein the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own modified address packet (Alan describes that cache tags represent the actual state of the data in the cache and consequently they transition with the data transfer or data modification (page 4, sec. 4.3 and 4.3.1). Since data is being transferred to the home node for write back the state should be invalid, which would relinquish ownership) and to responsively send a data packet corresponding to the coherency unit to the interface (Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to

write the coherency unit back (responsively send an additional coherency message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169])).

Regarding claims 9, 23 and 36, Alan in view of Jim and Hagersten describe the system of claim 8 (see above), the node of claim 22 (see above) and the method of claim 35 (see above), wherein the active device is configured to transition an access right corresponding to the coherency unit upon sending the data packet (Alan describes that cache tags represent the actual state of the data in the cache and consequently they transition with the data transfer or data modification (page 4, sec. 4.3 and 4.3.1). Since data is being transferred to the home node for write back the state should be invalid, which would relinquish ownership as well as current access right).

Regarding claim 20, Alan in view of Jim describe the node of claim 19 (see above). While they do describe a remote write back transaction, they do not specifically describe wherein a home interface in the home node is to responsively send a responsive coherency message for the coherency unit to the interface in the node wherein the interface in the node is configured to send a proxy read-to-own-modified address packet on the address network.

Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to write the coherency unit back (responsive

coherency message). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169]). In order to pass the coherency unit to the home node it must have been retrieved from the active device that contained the data using a request (proxy read-to-own-modified address packet) Alan describes the interfaces used to send and receive such inter-node messages (SSM Agents of Alan FIG. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the steps for accomplishing a write back as described by Hagersten with the invention of Alan in view of Jim because Hagersten shows that a write back request is performed in such a way (page 13, paragraph [0169]).

6. Claims 10 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alan in view of Jim and McCracken as applied to claims 2 and 29 above, further in view of Hagersten and Nishtala et al. US Patent No. 5581729 (herein after referred to as Nishtala).

Regarding claims 10 and 37, Alan in view of Jim and McCracken describe the system of claim 2 (see above) and the method of claim 29 (see above). They do not specifically describe the situation that if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive address packet the active device is configured to send a NACK data packet to the memory subsystem.

Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to write the coherency unit back (responsive address packet). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169]). Alan describes the interfaces used to send and receive such inter-node messages (SSM Agents of Alan FIG. 3). Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention that whatever device contains (has ownership) of the data to be written back should be the device to provide that data when it is to be written back.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the steps for accomplishing a write back as described by Hagersten with the invention of Alan in view of Jim and McCracken because Hagersten shows that a write back request is performed in such a way (page 13, paragraph [0169]). They still do not describe sending a NACK data packet to the memory subsystem.

Nishtala describes that if when the results (responsive address packet) of the snoop (WB address packet) for the transaction are received, if the Dtag corresponding for the specified address in the writeback transaction request is invalid, that means another data processor has performed a transaction that required invalidation of the address data block. When this happens, the writeback transaction is cancelled by the system controller by sending a

writeback cancel replay message (NACK) to the requesting UPA port (column 23, lines 18 – 29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have sent a NACK as described by Nishtala in the invention of Alan in view of Jim, McCracken and Hagersten because Nishtala shows that the writeback has become unnecessary and therefore should be cancelled (column 23, lines 18 - 29).

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alan in view of Jim as applied to claim 16 above, further in view of Hagersten and Nishtala et al. US Patent No. 5581729 (herein after referred to as Nishtala).

Regarding claim 24, Alan in view of Jim describe the node of claim 17 (see above). They do not specifically describe the situation that if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive address packet the active device is configured to send a NACK data packet to the memory subsystem.

Hagersten describes that a write back request is performed when a coherency unit is to be written to the home node of the coherency unit. The home node replies with permission to write the coherency unit back (responsive address packet). The coherency unit is then passed to the home node with the coherency completion (page 13, paragraph [0169]). Alan describes the interfaces used to send and receive such inter-node messages (SSM Agents of

Alan FIG. 3). Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention that whatever device contains (has ownership) of the data to be written back should be the device to provide that data when it is to be written back.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the steps for accomplishing a write back as described by Hagersten with the invention of Alan in view of Jim because Hagersten shows that a write back request is performed in such a way (page 13, paragraph [0169]). They still do not describe sending a NACK data packet to the memory subsystem.

Nishtala describes that if when the results (responsive address packet) of the snoop (WB address packet) for the transaction are received, if the Dtag corresponding for the specified address in the writeback transaction request is invalid, that means another data processor has performed a transaction that required invalidation of the address data block. When this happens, the writeback transaction is cancelled by the system controller by sending a writeback cancel replay message (NACK) to the requesting UPA port (column 23, lines 18 – 29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have sent a NACK as described by Nishtala in the invention of Alan in view of Jim and Hagersten because Nishtala shows that the writeback

has become unnecessary and therefore should be cancelled (column 23, lines 18 - 29).

8. Claims 11, 25 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alan in view of Jim as applied to claims 1, 16 and 28 above, further in view of Baxter et al. US Patent No. 5887146 (herein after referred to as Baxter) and Martin et al. "Bandwidth Adaptive Snooping" (herein after referred to as Martin).

Regarding claims 11, 25 and 38, Alan in view of Jim describes the system of claim 1 (see above), the node of claim 16 (see above) and the method of claim 28 (see above) but does not disclose the use of a mode register.

Martin, which describes snoop protocols, discloses the use of a counter to determine how many nodes are being used in the system (Martin Page 2).

Baxter, which describes a multi-node system, discloses the use of a mode register (Baxter, column 47, line 66).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a mode register to determine if the node is in a multi-node system because it is important to know the network utilization (Martin Page 2) and mode registers are well known and conventional in the art.

Response to Arguments

Applicant's arguments with respect to claims 1, 16 and 28 have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendment.

Applicant argues that dependent claims from 1, 16 and 28 are allowable for similar reasons that their independent claims are allowable. Examiner refers to rejections and response to arguments above as to why those claims are not allowable.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-Th 7:30 - 5, every other Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ralph A Verderamo III/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

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January 27, 2009